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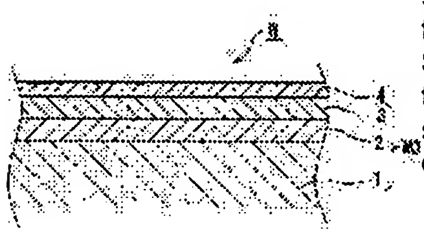
(54) **SEMICONDUCTOR SUBSTRATE, FIELD EFFECT TRANSISTOR, METHOD FOR FORMING SILICON-GERMANIUM LAYER, METHOD FOR FORMING STRAINED SILICON LAYER USING THE METHOD AND METHOD FOR MANUFACTURING FIELD EFFECT TRANSISTOR**



(57)Abstract:
PROBLEM TO BE SOLVED: To reduce the threading dislocation density of a SiGe layer in a method for forming a semiconductor substrate, field effect transistor and SiGe layer, a method for forming strained Si layer using this method, and a method for manufacturing a field effect transistor.
SOLUTION: The semiconductor substrate has SiGe layers 2 and 3 on the Si substrate 1. The crystal surface of the Si substrate is an off-cut surface that inclines from the plane direction (001) toward the crystal direction <100>.

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CLAIMS

[Claim(s)]
[Claim 1] It is the semiconductor substrate which is equipped with Si substrate and the SiGe layer on this Si substrate, and is characterized by the aforementioned Si substrate being a substrate which is the off-cut side where the crystal front face inclined from the field direction (001) side to the direction of crystal orientation <100>.
[Claim 2] It is the semiconductor substrate characterized by the degree of tilt angle of the aforementioned off-cut side being 10 degrees or less in a semiconductor substrate according to claim 1.
[Claim 3] It is the semiconductor substrate characterized by having the inclination composition field which the aforementioned SiGe layer turns germanium composition ratio to a front face in part at least in a semiconductor substrate according to claim 1 or 2, and increases gradually.
[Claim 4] The semiconductor substrate characterized by the thing which either of the claims 1-3 was matched through other direct or SiGe(s) layer on the aforementioned SiGe layer of the semiconductor substrate of a publication, and for which it was distorted and has Si layer.
[Claim 5] The field effect transistor which is a field effect transistor which has a channel field in the distortion Si layer on a SiGe layer, and is characterized by having the aforementioned channel field in the aforementioned distortion Si layer of a semiconductor substrate according to claim 4.
[Claim 6] The formation method of the SiGe layer which is the method of growing a SiGe layer epitaxially on Si substrate, and is characterized by using the aforementioned Si substrate as the substrate which is the off-cut side where the crystal front face inclined from the field direction (001) side to the direction of crystal orientation <100>.
[Claim 7] The formation method of the SiGe layer characterized by making the degree of tilt angle of the aforementioned off-cut side into 10 degrees or less in the formation method of a SiGe layer according to claim 6.
[Claim 8] The formation method of the SiGe layer characterized by forming the inclination composition field to which turned germanium composition ratio to the front face, and it was made to increase gradually in part at least among the aforementioned SiGe layers in the formation method of a SiGe layer according to claim 6 or 7.
[Claim 9] The formation method of the distortion Si layer which is the method which is distorted through a SiGe layer and forms Si layer on Si substrate, and is characterized by forming membranes by the formation method of a SiGe layer given [the SiGe layer on the aforementioned Si substrate] in either of the claims 6-8.
[Claim 10] The manufacture method of the field effect transistor which is the manufacture method of a field effect transistor which grew epitaxially on the SiGe layer that it is distorted and a channel field is formed in Si layer, and is characterized by forming the aforementioned distortion Si layer by the formation method of a distortion Si layer according to claim 9.
[Claim 11] The semiconductor substrate which is a semiconductor substrate by which the SiGe layer was formed on Si substrate, and is characterized by forming the aforementioned SiGe layer in either of the claims 6-8 by the formation method of the SiGe layer a publication.
[Claim 12] The semiconductor substrate which is a semiconductor substrate which is distorted through a SiGe layer, and by which Si layer was formed on Si substrate, and is characterized by forming the aforementioned distortion Si layer by the formation method of a distortion Si layer according to claim 9.
[Claim 13] The field effect transistor which is a distorted field effect transistor which grew epitaxially on the SiGe layer, and by which a channel field is formed in Si layer, and is characterized by forming the aforementioned distortion Si layer by the formation method of a distortion Si layer according to claim 9.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] this invention relates to the semiconductor substrate used for high-speed MOSFET etc., a field effect transistor, the formation method of a SiGe layer suitable in order to be distorted and to form Si layer etc., and the formation method of a distortion Si layer and the manufacture method of a field effect transistor using this.
[0002]
[Description of the Prior Art] In recent years, high-speed MOSFET which grew epitaxially through the SiGe (silicon germanium) layer on Si (silicon) substrate and which was distorted and used Si layer for the channel field, MODFET, and HEMT are proposed. In this distortion Si-FET, compared with Si, SiGe with a large lattice constant pulls in Si layer, and distortion arises, therefore the band structure of Si changes, degeneracy is cleared, and carrier mobility increases. Therefore, improvement in the speed of about 1.5 to 8 usual times is attained by using this distortion Si layer as a channel field. Moreover, as a process, the usual Si substrate by the CZ process can be used as a substrate, and realization of high-speed CMOS of it is enabled at the conventional CMOS process.
[0003] However, although the good SiGe layer needed to be grown epitaxially on Si substrate in order to have grown epitaxially the above-mentioned distortion Si layer demanded as a channel field of FET, the problem was in crystallinity by transposition etc. from the difference in the lattice constant of Si and SiGe. For this reason, the following various proposals were performed conventionally.
[0004] For example, the method using the buffer layer to which germanium composition ratio of SiGe was changed by the loose fixed inclination, The method using the buffer layer to which germanium (germanium) composition ratio was changed in the shape of a step (stair-like), germanium composition ratio The buffer layer changed in the shape of a superlattice The off-cut wafer of the method and Si to be used The method using the buffer layer to which it used for and germanium composition ratio was changed by the fixed inclination etc. is proposed (U. S.Patent 5,442,205, U.S.Patent 5,221,413, PCT WO 98/00857, JP,6-252046,A, etc.).
[0005] With the technology using the off-cut wafer of Si, the substrate which gave the off-cut toward which the crystal face (001) inclined to crystal orientation <110> is used among the above (81 PCTWO 98/00857, S.B.Samavedam and E.A.Fitzgerald, and J.Appl.Phys. Vol. 3108 (1997)). With this technology, in case two or more transposition generated during epitaxial growth of a SiGe film is extended in the inclination direction, it is not parallel at the step of a crystal and two or more transposition by the interaction of transposition can be bundled by using the property aslant extended with an inclination and making transposition cross. For this reason, the transposition of the inclination direction gathers, it becomes a bunch, and the penetration dislocation density in a front face is reduced as a result.
[0006]
[Problem(s) to be Solved by the Invention] However, the following technical problems are left behind in the above-mentioned Prior art. That is, in the above-mentioned Prior art, the penetration dislocation density on the front face of a wafer is still high, and in order to prevent the malfunction of a transistor, reduction of penetration transposition is demanded further. Although transposition converged and was especially reduced in the inclination direction (namely, the level difference direction of a crystal) with the above-mentioned conventional technology using the off-cut substrate of Si, since transposition runs in parallel and was not reduced towards not inclining, as a whole, the reduction effect of penetration dislocation density is low, and it was hard to reduce the density of the irregularity of the front face called cross hatching.
[0007] this invention was made in view of the above-mentioned technical problem, and aims at the thing which used the formation method of the semiconductor substrate and field effect transistor which can reduce the penetration dislocation density of a SiGe layer more, and a SiGe layer, and this and for which it is distorted and the formation method of Si layer and the manufacture method of a field effect transistor are offered.
[0008]
[Means for Solving the Problem] The following composition was used for this invention in order to solve the aforementioned technical problem. That is, the semiconductor substrate of this invention is equipped with Si substrate and the SiGe layer on this Si substrate, and the aforementioned Si substrate

is characterized by being the substrate which is the off-cut side where the crystal front face inclined from the field direction (001) side to the direction of crystal orientation <100>. Moreover, the formation method of the SiGe layer of this invention is the method of growing a SiGe layer epitaxially on Si substrate, and is characterized by using the aforementioned Si substrate as the substrate which is the off-cut side where the crystal front face inclined from the field direction (001) side to the direction of crystal orientation <100>. Moreover, the semiconductor substrate of this invention is a semiconductor substrate by which the SiGe layer was formed on Si substrate, and is characterized by forming the aforementioned SiGe layer by the formation method of the SiGe layer of the above-mentioned this invention.
[0009] By the formation method of these semiconductor substrates and a SiGe layer Since Si substrate is used as the substrate which is the off-cut side where the crystal front face inclined from the field direction (001) side to the direction (the direction [as opposed to / the <110> directions / Namely,] of 45 degrees of slant) of crystal orientation <100> In case the dislocation generated during SiGe layer membrane formation is extended in the <110> directions, it has an inclination to both two <110> directions which intersect perpendicularly under the influence of an off-cut, and the dislocation which runs in which direction also crosses mutually, and converges. That is, since the step of a crystal exists by the above-mentioned off-cut, in both of the directions, dislocation becomes less parallel, they cross and both the inclination direction and the direction which does not incline serve as a bunch of dislocation. For this reason, while dislocation density decreases on the whole and being able to reduce penetration dislocation density more, cross hatching nearby reduction can be carried out.
[0010] As for the semiconductor substrate of this invention, it is desirable that the degree of tilt angle of the aforementioned off-cut side is 10 degrees or less. Moreover, as for the formation method of the SiGe layer of this invention, it is desirable to make the degree of tilt angle of the aforementioned off-cut side into 10 degrees or less.
[0011] By the formation method of these semiconductor substrates and a SiGe layer, it can prevent an off-cut angle being too large and a crystal property changing a lot by making the degree of tilt angle of an off-cut side into 10 degrees or less. In addition, it is more desirable that an off-cut angle is within the limits from 6 degrees to 8 degrees. That is, it is because intersection of dislocation can be effectively generated if an off-cut angle is 6 degrees or more, and the same crystal property as a substrate (it is an parallel substrate to a crystal-face direction (001) side) is maintainable just if an off-cut angle is 8 degrees or less.
[0012] As for the semiconductor substrate of this invention, it is desirable to have the inclination composition field which the aforementioned SiGe layer turns germanium composition ratio to a front face in part at least, and increases gradually. Moreover, as for the formation method of the SiGe layer of this invention, it is desirable to form the inclination composition field to which turned germanium composition ratio to the front face, and it was made to increase gradually in part at least among the aforementioned SiGe layers.
[0013] By the formation method of these semiconductor substrates and a SiGe layer Since it considers as the inclination composition field to which at least the part turned germanium composition ratio to the front face, and made it increase gradually among SiGe layers In order that germanium composition ratio may increase gradually in an inclination composition field, penetration dislocation density can be further reduced by the synergistic effect with the dislocation convergence effect by Si substrate in a SiGe layer which could suppress the density of dislocation especially by the front-face side, and carried out the off-cut.
[0014] The semiconductor substrate of this invention is characterized by the thing which were matched through other direct or SiGe(s) layer on the aforementioned SiGe layer of the semiconductor substrate of the above-mentioned this invention and for which it was distorted and has Si layer. Moreover, the formation method of the distortion Si layer of this invention is a method which is distorted through a SiGe layer and forms Si layer on Si substrate, and is characterized by forming the SiGe layer on the aforementioned Si substrate by the formation method of the SiGe layer of the above-mentioned this invention. Moreover, the semiconductor substrate of this invention is a semiconductor substrate which is distorted through a SiGe layer and by which Si layer was formed on Si substrate, and is characterized by forming the aforementioned distortion Si layer by the formation method of the distortion Si layer of the above-mentioned this invention.

[0015] In the above-mentioned semiconductor substrate, it has the distortion Si layer allotted through other direct or SiGe(s) layer on the aforementioned SiGe layer of the semiconductor substrate of the above-mentioned this invention. by the formation method of the above-mentioned distortion Si layer The SiGe layer on Si substrate is formed by the formation method of the SiGe layer of the above-mentioned this invention. in the above-mentioned semiconductor substrate Since it is distorted by the formation method of the distortion Si layer of the above-mentioned this invention and Si layer is formed, it is suitable as the distortion Si layer or semiconductor substrate for integrated circuits using MOSFET which makes a distortion Si layer a channel field, for example.
[0016] The field effect transistor of this invention is a field effect transistor which has a channel field in the distortion Si layer on a SiGe layer, and is characterized by having the aforementioned channel field in the aforementioned distortion Si layer of the semiconductor substrate of the above-mentioned this invention. Moreover, the manufacture method of the field effect transistor of this invention is the manufacture method of a field effect transistor which grew epitaxially on the SiGe layer that it is distorted and a channel field is formed in Si layer, and is characterized by forming the aforementioned distortion Si layer by the formation method of the distortion Si layer of the above-mentioned this invention. Moreover, the field effect transistor of this invention is a distorted field effect transistor which grew epitaxially on the SiGe layer and by which a channel field is formed in Si layer, and is characterized by forming the aforementioned distortion Si layer by the formation method of the distortion Si layer of the above-mentioned this invention.
[0017] since it has the aforementioned channel field in the above-mentioned field effect transistor in the aforementioned distortion Si layer of the semiconductor substrate of the above-mentioned this invention, the aforementioned distortion Si layer forms by the formation method of the distortion Si layer of the above-mentioned this invention by the manufacture method of the above-mentioned field effect transistor and the aforementioned distortion Si layer is formed by the formation method of the distortion Si layer of the above-mentioned this invention in the above-mentioned field effect transistor -- a good distortion Si layer -- high -- a property electric field effect type transistor can obtain by the high yield
[0018]
[Embodiments of the Invention] Hereafter, 1 operation form concerning this invention is explained, referring to drawing 1 and drawing 2 .
[0019] Drawing 1 is what shows the cross-section structure of the semiconductor wafer (semiconductor wafer) W equipped with the semiconductor wafer (semiconductor wafer) W0 and distortion Si layer of this invention. If the structure of the semiconductor wafer W equipped with this semiconductor wafer W0 and the distortion Si layer is explained together with the manufacture process, as shown in drawing 1 and drawing 2 , first The 1st SiGe layer 2 which is the inclination composition layer which germanium composition ratio x has an inclination (turning to a front face) in the membrane formation direction, and increases gradually from 0 to 0.3 on the Si substrate 1 is grown epitaxially by reduced pressure CVD. In addition, the membrane formation by the above-mentioned reduced pressure CVD uses SiH4 and GeH4 as source gas, using H2 as carrier gas.
[0020] next, the 1st SiGe layer 2 top -- this -- the 2nd SiGe layer 3 which is a fixed composition layer and a relief layer in final germanium composition ratio (0.3) of the 1st SiGe layer 2 is grown epitaxially, and the semiconductor wafer W0 is manufactured These 1st SiGe layer 2 and the 2nd SiGe layer 3 function as SiGe layers for forming a distortion Si layer.
[0021] Thus, since the 2nd SiGe layer 3 of a fixed composition layer is formed after forming the 1st SiGe layer 2 of an inclination composition layer, generating and growth of the dislocation in the 2nd SiGe layer 3 can be suppressed, and the dislocation density of the 2nd SiGe layer 3 final front face can be reduced. Furthermore, on the 2nd [of this semiconductor wafer W0] SiGe layer 3, Si is grown epitaxially and distorted, the Si layer 4 is formed, and the semiconductor wafer W equipped with the distortion Si layer is produced. In addition, for the 1st SiGe layer 2, 1.5 micrometers and the 2nd SiGe layer 3 are [0.75 micrometers and the distortion Si layer 4 of the thickness of each class] 15-22nm.
[0022] The substrate which is the off-cut side where the crystal front face inclined from the field direction (001) side to the direction of crystal orientation <100>, i.e., the <110> directions, as the above-mentioned Si substrate 1 to the <100> directions which are the direction of 45 degrees of slant is used. Moreover, the degree of tilt angle of an off-cut side is made into 10 degrees or less, and is desirably set up between 6 degrees and 8 degrees.

[0023] in addition, a field direction (001) -- it is equivalent to and (100) (010) Moreover, crystal orientation <100> is the general term of 6 crystal orientation of [100], [-100], [010], [0-10], [001], and [00-1], and is equivalent to <010> and <001>. Moreover, crystal orientation <110> is the general term of [110], [101], [011], [-110], [-101], [0-11], [1-10], [10-1], [01-1], [-1-10], [-10-1], and [0-1-1], and is equivalent to <011> and <101>. Then, <100> and <110> are taken as these general terms in this invention (001). In addition, for convenience, such crystal orientation has indicated ICHIBA, zero, and zero, as shown in [-100].
[0024] Since the Si substrate 1 is used as the substrate which is the off-cut side where the crystal front face inclined from the field direction (001) side to the direction of crystal orientation <100> with this operation form In case the dislocation generated during SiGe layer membrane formation runs in the <110> directions, it has an inclination to both two <110> directions which intersect perpendicularly under the influence of an off-cut, and dislocation becomes less parallel, they cross and the dislocation extended in which direction also serves as a bunch of dislocation. For this reason, while dislocation density decreases on the whole and being able to reduce penetration dislocation density more, cross hatching nearby reduction can be carried out.
[0025] Moreover, when an off-cut angle is within the limits from 6 degrees to 8 degrees, while being able to prevent an off-cut angle being too large and a crystal property changing a lot by making the degree of tilt angle of an off-cut side into 10 degrees or less and being able to generate intersection of dislocation effectively further, the same crystal property as a substrate is maintainable just.
[0026] Furthermore, in order that germanium composition ratio may increase gradually in the 1st SiGe layer 2 which is an inclination composition field, the density of the dislocation in the 2nd SiGe layer 3 can be suppressed, and penetration dislocation density can be further reduced by the synergistic effect with the dislocation convergence effect by the Si substrate 1 of an off-cut substrate.
[0027] Next, the field effect transistor (MOSFET) using the semiconductor wafer W equipped with the above-mentioned distortion Si layer of this invention is explained with reference to drawing 3 together with the manufacture process.
[0028] Drawing 3 deposits the gate oxide film 5 of SiO2, and the gate polysilicon contest film 6 one by one on the distortion Si layer 4 of the semiconductor wafer W front face which was produced by the above-mentioned manufacturing process and which was distorted and was equipped with Si layer, in order to show the rough structure of the field effect transistor of this invention and to manufacture this field effect transistor. And on the gate polysilicon contest film 6 on the portion used as a channel field, patterning of the gate electrode (illustration abbreviation) is carried out, and it is formed.
[0029] Next, patterning also of the gate oxide film 5 is carried out, and it removes portions other than under a gate electrode. Furthermore, n type or the p type source field S, and the drain field D are formed in the distortion Si layer 4 and the 2nd SiGe layer 3 with the ion implantation which used the gate electrode for the mask at a self-adjustment target. Then, a source electrode and a drain electrode (illustration abbreviation) are formed on the source field S and the drain field D, respectively, and n type or p type MOSFET from which the distortion Si layer 4 serves as a channel field is manufactured.
[0030] Thus, at produced MOSFET, since a channel field is formed in the distortion Si layer 4 on the semiconductor wafer W which was produced by the above-mentioned process and which was distorted and was equipped with Si layer, MOSFET which was excellent in the operating characteristic with the good distortion Si layer 4 can be obtained by the high yield.
[0031] in addition, the technical range of this invention can add various change in the range which is not limited to the gestalt of the above-mentioned implementation and does not deviate from the meaning of this invention For example, the semiconductor wafer further equipped with the SiGe layer on the distortion Si layer of the semiconductor wafer W equipped with the distortion Si layer of the above-mentioned operation gestalt is also contained in this invention. Moreover, although the distortion Si layer was directly formed on the 2nd SiGe layer, on the 2nd SiGe layer, the SiGe layer of further others may be formed, it may be distorted through this SiGe layer, and you may grow Si layer epitaxially.
[0032] Moreover, the above-mentioned operation gestalt is available also as a substrate applied to other uses, although the semiconductor wafer which has a SiGe layer as a substrate for MOSFET was produced. For example, you may apply the formation method of the SiGe layer of this invention, and a semiconductor substrate to the substrate for solar batteries. That is, you may produce the substrate for solar batteries by forming the SiGe layer of the inclination composition layer to which germanium

composition ratio was made to increase gradually so that it may become germanium 100% on the maximum front face on Si substrate of the operation gestalt mentioned above, and forming GaAs (gallium arsenide) on this further. In this case, the substrate for solar batteries of the high property in low dislocation density is obtained.
[0033]
[Effect of the Invention] According to this invention, the following effects are done so. Since Si substrate is used as the substrate which is the off-cut side where the crystal front face inclined from the field direction (001) side to the direction of crystal orientation <100> according to the formation method of the semiconductor substrate of this invention, and a SiGe layer The transposition extended in which direction of the two <110> directions which intersect perpendicularly also crosses, and it becomes the bunch of transposition, and while dislocation density decreases on the whole and being able to reduce penetration dislocation density more, cross hatching nearby reduction can be carried out.
[0034] Moreover, since Si substrate in which membranes are formed by the formation method of the SiGe layer of the above-mentioned this invention, and the SiGe layer on Si substrate has a SiGe layer is a semiconductor substrate of the above-mentioned this invention according to the formation method of the semiconductor substrate equipped with the distortion Si layer of this invention, and a distortion Si layer, on a good SiGe layer, a surface state can form Si layer and can form a good distortion Si layer.
[0035] moreover -- since according to the manufacture method of the field effect transistor of this invention, and a field effect transistor the distortion Si layer used as a channel field is formed or the channel field is formed in the aforementioned distortion Si layer of the semiconductor substrate of the above-mentioned this invention by the formation method of the distortion Si layer of the above-mentioned this invention -- a good distortion Si layer -- high -- property MOSFET can be obtained by the high yield

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[Translation done.]

TECHNICAL FIELD

[The technical field to which invention belongs] this invention relates to the semiconductor substrate used for high-speed MOSFET etc., a field effect transistor, the formation method of a SiGe layer suitable in order to be distorted and to form Si layer etc., and the formation method of a distortion Si layer and the manufacture method of a field effect transistor using this.

[Translation done.]

PRIOR ART

[Description of the Prior Art] In recent years, high-speed MOSFET which grew epitaxially through the SiGe (silicon germanium) layer on Si (silicon) substrate and which was distorted and used Si layer for the channel field, MODFET, and HEMT are proposed. In this distortion Si-FET, compared with Si, SiGe with a large lattice constant pulls in Si layer, and distortion arises, therefore the band structure of Si changes, degeneracy is cleared, and carrier mobility increases. Therefore, improvement in the speed of about 1.5 to 8 usual times is attained by using this distortion Si layer as a channel field. Moreover, as a process, the usual Si substrate by the CZ process can be used as a substrate, and realization of high-speed CMOS of it is enabled at the conventional CMOS process.
[0003] However, although the good SiGe layer needed to be grown epitaxially on Si substrate in order to have grown epitaxially the above-mentioned distortion Si layer demanded as a channel field of FET, the problem was in crystallinity by dislocation etc. from the difference in the lattice constant of Si and SiGe. For this reason, the following various proposals were performed conventionally.
[0004] For example, germanium composition ratio of SiGe. The method using the buffer layer changed

by the loose fixed inclination, the method using the buffer layer to which germanium (germanium) composition ratio was changed in the shape of a step (stair-like), germanium composition ratio The buffer layer changed in the shape of a superlattice The off-cut wafer of the method and Si to be used The method using the buffer layer to which it used for and germanium composition ratio was changed by the fixed inclination etc. is proposed (U. S.Patent 5,442,205, U.S.Patent 5,221,413, PCT WO 98/00857, JP,6-252046,A, etc.).
[0005] With the technology using the off-cut wafer of Si, the substrate which gave the off-cut toward which the crystal face (001) inclined to crystal orientation <110> is used among the above (81 PCTWO 98/00857, S.B.Samavedam and E.A.Fitzgerald, and J.Appl.Phys. Vol. 3108 (1997)). With this technology, in case two or more transposition generated during epitaxial growth of a SiGe film is extended in the inclination direction, it is not parallel at the step of a crystal and two or more transposition by the interaction of transposition can be bundled by using the property aslant extended with an inclination and making transposition cross. For this reason, the transposition of the inclination direction gathers, it becomes a bunch, and the penetration dislocation density in a front face is reduced as a result.

[Translation done.]

EFFECT OF THE INVENTION

[Effect of the Invention] According to this invention, the following effects are done so. Since Si substrate is used as the substrate which is the off-cut side where the crystal front face inclined from the field direction (001) side to the direction of crystal orientation <100> according to the formation method of the semiconductor substrate of this invention, and a SiGe layer The dislocation extended in which direction of the two <110> directions which intersect perpendicularly also crosses, and it becomes the bunch of dislocation, and while dislocation density decreases on the whole and being able to reduce penetration dislocation density more, cross hatching nearby reduction can be carried out.
[0034] Moreover, since Si substrate in which membranes are formed by the formation method of the SiGe layer of the above-mentioned this invention, and the SiGe layer on Si substrate has a SiGe layer is a semiconductor substrate of the above-mentioned this invention according to the formation method of the semiconductor substrate equipped with the distortion Si layer of this invention, and a distortion Si layer, on a good SiGe layer, a surface state can form Si layer and can form a good distortion Si layer.
[0035] moreover -- since according to the manufacture method of the field effect transistor of this invention, and a field effect transistor the distortion Si layer used as a channel field is formed or the channel field is formed in the aforementioned distortion Si layer of the semiconductor substrate of the above-mentioned this invention by the formation method of the distortion Si layer of the above-mentioned this invention -- a good distortion Si layer -- high -- property MOSFET can be obtained by the high yield

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[Translation done.]

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] However, the following technical problems are left behind in the above-mentioned Prior art. That is, in the above-mentioned Prior art, the penetration dislocation density on the front face of a wafer is still high, and in order to prevent the malfunction of a transistor, reduction of penetration dislocation is demanded further. Although dislocation converged and was especially reduced in the inclination direction (namely, the level difference direction of a crystal) with the above-mentioned conventional technology using the off-cut substrate of Si, since dislocation ran in parallel and was not reduced towards not inclining, as a whole, the reduction effect of penetration

dislocation density is low, and it was hard to reduce the density of the irregularity of the front face called cross hatching.
[0007] this invention was made in view of the above-mentioned technical problem, and aims at the thing which used the formation method of the semiconductor substrate and field effect transistor which can reduce the penetration dislocation density of a SiGe layer more, and a SiGe layer, and this and for which it is distorted and the formation method of Si layer and the manufacture method of a field effect transistor are offered.

[Translation done.]

MEANS

[Means for Solving the Problem] The following composition was used for this invention in order to solve the aforementioned technical problem. That is, the semiconductor substrate of this invention is equipped with Si substrate and the SiGe layer on this Si substrate, and the aforementioned Si substrate is characterized by being the substrate which is the off-cut side where the crystal front face inclined from the field direction (001) side to the direction of crystal orientation <100>. Moreover, the formation method of the SiGe layer of this invention is the method of growing a SiGe layer epitaxially on Si substrate, and is characterized by using the aforementioned Si substrate as the substrate which is the off-cut side where the crystal front face inclined from the field direction (001) side to the direction of crystal orientation <100>. Moreover, the semiconductor substrate of this invention is a semiconductor substrate by which the SiGe layer was formed on Si substrate, and is characterized by forming the aforementioned SiGe layer by the formation method of the SiGe layer of the above-mentioned this invention.
[0009] By the formation method of these semiconductor substrates and a SiGe layer Since Si substrate is used as the substrate which is the off-cut side where the crystal front face inclined from the field direction (001) side to the direction (the direction [as opposed to / the <110> directions / Namely,] of 45 degrees of slant) of crystal orientation <100> In case the transposition generated during SiGe layer membrane formation is extended in the <110> directions, it has an inclination to both two <110> directions which intersect perpendicularly under the influence of an off-cut, and the transposition which runs in which direction also crosses mutually, and converges. That is, since the step of a crystal exists by the above-mentioned off-cut, in both of the directions, transposition becomes less parallel, they cross and both the inclination direction and the direction which does not incline serve as a bunch of transposition. For this reason, while dislocation density decreases on the whole and being able to reduce penetration dislocation density more, cross hatching nearby reduction can be carried out.
[0010] As for the semiconductor substrate of this invention, it is desirable that the degree of tilt angle of the aforementioned off-cut side is 10 degrees or less. Moreover, as for the formation method of the SiGe layer of this invention, it is desirable to make the degree of tilt angle of the aforementioned off-cut side into 10 degrees or less.
[0011] By the formation method of these semiconductor substrates and a SiGe layer, it can prevent an off-cut angle being too large and a crystal property changing a lot by making the degree of tilt angle of an off-cut side into 10 degrees or less. In addition, it is more desirable that an off-cut angle is within the limits from 6 degrees to 8 degrees. That is, it is because intersection of transposition can be effectively generated if an off-cut angle is 6 degrees or more, and the same crystal property as a substrate (it is an parallel substrate to a crystal-face direction (001) side) is maintainable just if an off-cut angle is 8 degrees or less.
[0012] As for the semiconductor substrate of this invention, it is desirable to have the inclination composition field which the aforementioned SiGe layer turns germanium composition ratio to a front face in part at least, and increases gradually. Moreover, as for the formation method of the SiGe layer of this invention, it is desirable to form the inclination composition field to which turned germanium composition ratio to the front face, and it was made to increase gradually in part at least among the aforementioned SiGe layers.

[0013] By the formation method of these semiconductor substrates and a SiGe layer Since it considers as the inclination composition field to which at least the part turned germanium composition ratio to the front face, and made it increase gradually among SiGe layers In order that germanium composition ratio may increase gradually in an inclination composition field, penetration dislocation density can be further reduced by the synergistic effect with the transposition convergence effect by Si substrate in a SiGe layer which could suppress the density of transposition especially by the front-face side, and carried out the off-cut.
[0014] The semiconductor substrate of this invention is characterized by the thing which were matched through other direct or SiGe(s) layer on the aforementioned SiGe layer of the semiconductor substrate of the above-mentioned this invention and for which it was distorted and has Si layer. Moreover, the formation method of the distortion Si layer of this invention is a method which is distorted through a SiGe layer and forms Si layer on Si substrate, and is characterized by forming the SiGe layer on the aforementioned Si substrate by the formation method of the SiGe layer of the above-mentioned this invention. Moreover, the semiconductor substrate of this invention is a semiconductor substrate which is distorted through a SiGe layer and by which Si layer was formed on Si substrate, and is characterized by forming the aforementioned distortion Si layer by the formation method of the distortion Si layer of the above-mentioned this invention.
[0015] In the above-mentioned semiconductor substrate, it has the distortion Si layer allotted through other direct or SiGe(s) layer on the aforementioned SiGe layer of the semiconductor substrate of the above-mentioned this invention. by the formation method of the above-mentioned distortion Si layer The SiGe layer on Si substrate is formed by the formation method of the SiGe layer of the above-mentioned this invention. in the above-mentioned semiconductor substrate Since it is distorted by the formation method of the distortion Si layer of the above-mentioned this invention and Si layer is formed, it is suitable as the distortion Si layer or semiconductor substrate for integrated circuits using MOSFET which makes a distortion Si layer a channel field, for example.
[0016] The field effect transistor of this invention is a field effect transistor which has a channel field in the distortion Si layer on a SiGe layer, and is characterized by having the aforementioned channel field in the aforementioned distortion Si layer of the semiconductor substrate of the above-mentioned this invention. Moreover, the manufacture method of the field effect transistor of this invention is the manufacture method of a field effect transistor which grew epitaxially on the SiGe layer that it is distorted and a channel field is formed in Si layer, and is characterized by forming the aforementioned distortion Si layer by the formation method of the distortion Si layer of the above-mentioned this invention. Moreover, the field effect transistor of this invention is a distorted field effect transistor which grew epitaxially on the SiGe layer and by which a channel field is formed in Si layer, and is characterized by forming the aforementioned distortion Si layer by the formation method of the distortion Si layer of the above-mentioned this invention.
[0017] since it has the aforementioned channel field in the above-mentioned field effect transistor in the aforementioned distortion Si layer of the semiconductor substrate of the above-mentioned this invention, the aforementioned distortion Si layer forms by the formation method of the distortion Si layer of the above-mentioned this invention by the manufacture method of the above-mentioned field effect transistor and the aforementioned distortion Si layer is formed by the formation method of the distortion Si layer of the above-mentioned this invention in the above-mentioned field effect transistor -- a good distortion Si layer -- high -- a property electric field effect type transistor can obtain by the high yield
[0018]
[Embodiments of the Invention] Hereafter, 1 operation gestalt concerning this invention is explained, referring to drawing 1 and drawing 2 .
[0019] Drawing 1 is what shows the cross-section structure of the semiconductor wafer (semiconductor wafer) W equipped with the semiconductor wafer (semiconductor wafer) W0 and distortion Si layer of this invention. If the structure of the semiconductor wafer W equipped with this semiconductor wafer W0 and the distortion Si layer is explained together with the manufacture process, as shown in drawing 1 and drawing 2 , first The 1st SiGe layer 2 which is the inclination composition layer which germanium composition ratio x has an inclination (turning to a front face) in the membrane formation direction, and increases gradually from 0 to 0.3 on the Si substrate 1 is grown epitaxially by reduced pressure CVD. In addition, the membrane formation by the above-mentioned reduced pressure CVD uses SiH4 and

GeH4 as source gas, using H2 as carrier gas.
[0020] next, the 1st SiGe layer 2 top -- this -- the 2nd SiGe layer 3 which is a fixed composition layer and a relief layer in final germanium composition ratio (0.3) of the 1st SiGe layer 2 is grown epitaxially, and the semiconductor wafer W0 is manufactured These 1st SiGe layer 2 and the 2nd SiGe layer 3 function as SiGe layers for forming a distortion Si layer.
[0021] Thus, since the 2nd SiGe layer 3 of a fixed composition layer is formed after forming the 1st SiGe layer 2 of an inclination composition layer, generating and growth of the dislocation in the 2nd SiGe layer 3 can be suppressed, and the dislocation density of the 2nd SiGe layer 3 final front face can be reduced. Furthermore, on the 2nd [of this semiconductor wafer W0] SiGe layer 3, Si is grown epitaxially and distorted, the Si layer 4 is formed, and the semiconductor wafer W equipped with the distortion Si layer is produced. In addition, for the 1st SiGe layer 2, 1.5 micrometers and the 2nd SiGe layer 3 are [0.75 micrometers and the distortion Si layer 4 of the thickness of each class] 15-22nm.
[0022] The substrate which is the off-cut side where the crystal front face inclined from the field direction (001) side to the direction of crystal orientation <100>, i.e., the <110> directions, as the above-mentioned Si substrate 1 to the <100> directions which are the direction of 45 degrees of slant is used. Moreover, the degree of tilt angle of an off-cut side is made into 10 degrees or less, and is desirably set up between 6 degrees and 8 degrees.
[0023] in addition, a field direction (001) -- it is equivalent to and (100) (010) Moreover, crystal orientation <100> is the general term of 6 crystal orientation of [100], [-100], [010], [0-10], [001], and [00-1], and is equivalent to <010> and <001>. Moreover, crystal orientation <110> is the general term of [110], [101], [011], [-110], [-101], [0-11], [1-10], [10-1], [01-1], [-1-10], [-10-1], and [0-1-1], and is equivalent to <011> and <101>. Then, <100> and <110> are taken as these general terms in this invention (001). In addition, for convenience, such crystal orientation has indicated ICHIBA, zero, and zero, as shown in [-100].
[0024] Since the Si substrate 1 is used as the substrate which is the off-cut side where the crystal front face inclined from the field direction (001) side to the direction of crystal orientation <100> with this operation form In case the dislocation generated during SiGe layer membrane formation runs in the <110> directions, it has an inclination to both two <110> directions which intersect perpendicularly under the influence of an off-cut, and dislocation becomes less parallel, they cross and the dislocation extended in which direction also serves as a bunch of dislocation. For this reason, while dislocation density decreases on the whole and being able to reduce penetration dislocation density more, cross hatching nearby reduction can be carried out.
[0025] Moreover, when an off-cut angle is within the limits from 6 degrees to 8 degrees, while being able to prevent an off-cut angle being too large and a crystal property changing a lot by making the degree of tilt angle of an off-cut side into 10 degrees or less and being able to generate intersection of dislocation effectively further, the same crystal property as a substrate is maintainable just.
[0026] Furthermore, in order that germanium composition ratio may increase gradually in the 1st SiGe layer 2 which is an inclination composition field, the density of the dislocation in the 2nd SiGe layer 3 can be suppressed, and penetration dislocation density can be further reduced by the synergistic effect with the dislocation convergence effect by the Si substrate 1 of an off-cut substrate.
[0027] Next, the field effect transistor (MOSFET) using the semiconductor wafer W equipped with the above-mentioned distortion Si layer of this invention is explained with reference to drawing 3 together with the manufacture process.
[0028] Drawing 3 deposits the gate oxide film 5 of SiO2, and the gate polysilicon contest film 6 one by one on the distortion Si layer 4 of the semiconductor wafer W front face which was produced by the above-mentioned manufacturing process and which was distorted and was equipped with Si layer, in order to show the rough structure of the field effect transistor of this invention and to manufacture this field effect transistor. And on the gate polysilicon contest film 6 on the portion used as a channel field, patterning of the gate electrode (illustration abbreviation) is carried out, and it is formed.
[0029] Next, patterning also of the gate oxide film 5 is carried out, and it removes portions other than under a gate electrode. Furthermore, n type or the p type source field S, and the drain field D are formed in the distortion Si layer 4 and the 2nd SiGe layer 3 with the ion implantation which used the gate electrode for the mask at a self-adjustment target. Then, a source electrode and a drain electrode (illustration abbreviation) are formed on the source field S and the drain field D, respectively, and n type

or p type MOSFET from which the distortion Si layer 4 serves as a channel field is manufactured.
[0030] Thus, at produced MOSFET, since a channel field is formed in the distortion Si layer 4 on the semiconductor wafer W which was produced by the above-mentioned process and which was distorted and was equipped with Si layer, MOSFET which was excellent in the operating characteristic with the good distortion Si layer 4 can be obtained by the high yield.
[0031] in addition, the technical range of this invention can add various change in the range which is not limited to the form of the above-mentioned implementation and does not deviate from the meaning of this invention For example, the semiconductor wafer further equipped with the SiGe layer on the distortion Si layer of the semiconductor wafer W equipped with the distortion Si layer of the above-mentioned operation form is also contained in this invention. Moreover, although the distortion Si layer was directly formed on the 2nd SiGe layer, on the 2nd SiGe layer, the SiGe layer of further others may be formed, it may be distorted through this SiGe layer, and you may grow Si layer epitaxially.
[0032] Moreover, the above-mentioned operation form is available also as a substrate applied to other uses, although the semiconductor wafer which has a SiGe layer as a substrate for MOSFET was produced. For example, you may apply the formation method of the SiGe layer of this invention, and a semiconductor substrate to the substrate for solar batteries. That is, you may produce the substrate for solar batteries by forming the SiGe layer of the inclination composition layer to which germanium composition ratio was made to increase gradually so that it may become germanium 100% on the maximum front face on Si substrate of the operation form mentioned above, and forming GaAs (gallium arsenide) on this further. In this case, the substrate for solar batteries of the high property in low dislocation density is obtained.

[Translation done.]

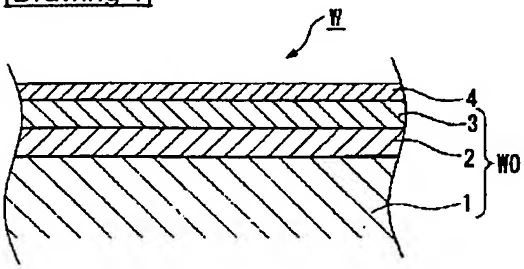
DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the cross section showing the semiconductor substrate equipped with the distortion Si layer in 1 operation gestalt concerning this invention.
[Drawing 2] It is the graph which shows germanium composition ratio to the thickness of the semiconductor substrate equipped with the distortion Si layer in 1 operation gestalt concerning this invention.
[Drawing 3] It is the rough cross section showing MOSFET in 1 operation gestalt concerning this invention.
[Description of Notations]
1 Si Substrate
2 1st SiGe Layer
3 2nd SiGe Layer
4 Distortion Si Layer
5 SiO2 Gate Oxide Film
6 Gate Polysilicon Contest Film
S Source field
D Drain field
W The semiconductor wafer equipped with the distortion Si layer (semiconductor substrate)
W0 Semiconductor wafer (semiconductor substrate)

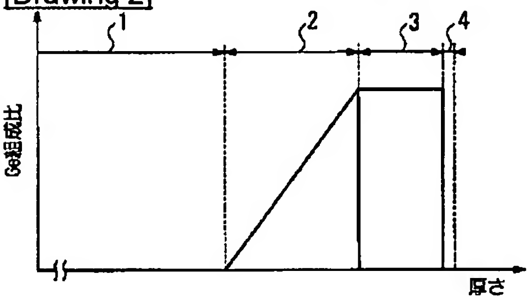
[Translation done.]

DRAWINGS

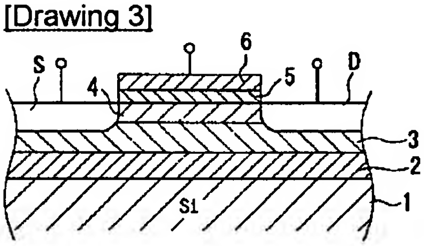
[Drawing 1]



[Drawing 2]



[Drawing 3]



[Translation done.]